## REMARKS

Claims 1-12 are pending in the present application. Claims 1 and 8 are amended above. No new matter is added by the claim amendments. Entry is respectfully requested.

Claims 1-12 are rejected as being anticipated by Haraguchi (U.S. Patent No. 5,469,391). Reconsideration of the rejections and allowance of the claims are respectfully requested.

The present invention of amended claim 1 is directed to a fuse circuit for a semiconductor integrated circuit. The fuse circuit includes a plurality of fuses; and a like plurality of transmission circuits. Each of the plurality of fuses is coupled to only one corresponding transmission circuit of the plurality of transmission circuits. Each transmission circuit transfers signals from an input node to an output node in response to a status of the corresponding fuse, the input and output nodes of respective transmission circuits being coupled such that the transmission circuits are arranged in series. In this manner, an input signal applied to the input node of a first transmission circuit in the series is transferred to the output node of a last transmission circuit in the series when all of the transmission circuits in the series are in an active state, and the input signal is not transferred from the input node of the first transmission circuit to the output node of the last transmission circuit in the series when at least one of the transmission circuits in the series is in an inactive state.

The present invention of amended claim 8 is directed to a fuse circuit storing information related to a semiconductor integrated circuit. The fuse circuit includes a plurality of fuses each of which has first and second terminals. The first terminal of each is connected to a power supply voltage. Each fuse stores predetermined information relevant to the semiconductor integrated circuit. The fuse circuit further includes a like plurality of transmission circuits. A second terminal of each of the plurality of fuses is coupled to only one corresponding transmission circuit of the plurality of transmission circuits. Each transmission circuit transfers an input signal received at an input terminal to an output terminal in response to the predetermined information established by a status of the corresponding fuse. The transmission

circuits are connected in series. In this manner, an input signal applied to the input terminal of a first transmission circuit in the series is transferred to the output terminal of a last transmission circuit in the series when all of the transmission circuits in the series are in an active state, and the input signal is not transferred from the input terminal of the first transmission circuit to the output terminal of the last transmission circuit in the series when at least one of the transmission circuits in the series is in an inactive state.

In the present invention as claimed in independent claim 1 , the "fuse circuit" includes "a plurality of fuses", and a "like plurality of transmission circuits". "Each of the plurality of fuses is "coupled to only one corresponding transmission circuit of the plurality of transmission circuits". Thus, each fuse of the "plurality of fuses" is coupled to a single, i.e. "only one" of the "like plurality of transmission circuits".

In the present invention as claimed in independent claim 8 , the "fuse circuit" includes "a plurality of fuses", and a "like plurality of transmission circuits". A second terminal of "each of the plurality of fuses" is connected to only one corresponding transmission circuit of the plurality of transmission circuits". Thus, each fuse of the "plurality of fuses" is coupled to a single, i.e. "only one" of the "like plurality of transmission circuits".

In this manner, the present invention utilizes a plurality of fuses for storing redundant, identical bit information. As a result, in the event that a fuse has not been cut correctly, the fuse circuit of the present invention nevertheless operates to drastically reduce programming defect rates.

In contrast, in Haraguchi, being directed to an address decoding circuit, each fuse 163, 263 is connected to more than one corresponding transmission gate TG11-TG14, TG21-TG24. For example, fuse 163 is connected to four transmission gates TG11-TG14. Since the Haraguchi embodiment is configured as a 2-to-4 (FIG. 17) or 3-to-8 (FIG. 18) decoder, in the case where a fuse has been erroneously cut, an undesired result (Sb) is output.

It is therefore submitted that Haraguchi fails to teach or suggest the present invention as claimed in amended independent claims 1 and 8. Reconsideration and removal of the rejection of independent claims 1 and 8, and the various claims dependent thereon, are therefore respectfully requested.

Closing Remarks

It is submitted that all claims are in condition for allowance, and such allowance is respectfully requested. If prosecution of the application can be expedited by a telephone conference, the Examiner is invited to call the undersigned at the number given below.

Respectfully submitted,

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